RF Effects of LCP on III-V HEMTs for 3DMMICs

Raytheon Funded Project

Final Report

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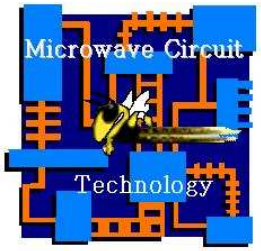


This report describes the collaborative activities between Georgia Tech and Raytheon for the Invariant MMIC project during the period October 2007 through October 2008. The research and development efforts under the University funded project can be directed in three major sub-tasks which are compiled in Sections I, II and III. Each section describes project objectives, project description, experimental procedure, data acquisition and interpretations, and finally a short conclusion on the sub-task level.

Section I. Hybrid Wafer Level Packaging

This section describes the feasibility study of a wafer level process where MMICs on a large wafer is covered with a low loss organic with laser micro-machined air cavity in the FET and the bond pad area. The RF performances before and after the air-cavity were evaluated for process qualification.

Introduction

With the rapid growth in wireless communications and the consistent need for low-cost high performance circuitry, it has become necessary to integrate RF circuits in a large processing format, the wafer level processing being the most attractive. However, integration of MMICs on a wafer level process requires additional layers of dielectric material for global interconnections and by doing so, performance of the MMICs will degrade due to the overlay of the dielectric layers on the semiconductor substrate. These dielectric materials are typically oxides, nitrides, polyimides or BCBs [1-3]. One of the issues with these materials is increased cost due to several processing steps as well as mechanical considerations, such as the CTE (coefficient of thermal expansion) mismatch between them and the semiconductor substrates, as well as higher loss in microwave and mm-wave bands. A low cost wafer level packaging technique for MMICs by using an organic substrate that can serve as host to a variety of passive circuits with very good performance, such as filters and antennas [4-6] has bee studied. The selected organic substrate is a liquid crystal polymer that provides the best electrical performance as a microwave dielectric material among the family of organic-based packaging materials and also has a CTE (3-30 ppm/C) that can be matched to that of Si or GaAs. Some of the niche advantages of the LCP are: Superior cost/performance index, flexibility for application in conformal flex circuits, lower permittivity and lower dielectric loss, minimum dispersion in permittivity and dielectric loss up to 110 GHz, low coefficient of thermal expansion (CTE), low moisture uptake, ease of multi-chip interconnect and processing, and X.Y,Z interconnect formation [7,8].

Traditionally, the LCP is processed in a multi-layered format similar to the printed wiring board process. However, process optimization can lead to good bonding to a silicon or GaAs wafer, thereby providing latitude for application as a dielectric material for the MMIC process integration. This paper takes advantage of the processing technologies perfected for bonding of wafers onto LCP. It presents a GaAs MMIC embedded in LCP layers. In this process, several LNAs are made on a six or eight inch GaAs wafer using wafer level process. A blank LCP layer

(25 to 100 micron in thickness) is then laminated on the entire wafer with pre-cut windows thus creating an air-cavity in the active part of the entire wafer. RF performance was measured before and after the LCP lamination.

Fabrication

The test chips are single stage amplifiers as shown in Figure 1. This microstrip MMIC consists of FETs, an input matchingband output matching network designed for 50 ohms. The matching network topology uses microstrip lines and MIM capacitors. The dotted area represents the FET and bond-pads which are to be opened by laser ablation through the LCP layer to access the pads for measurement.

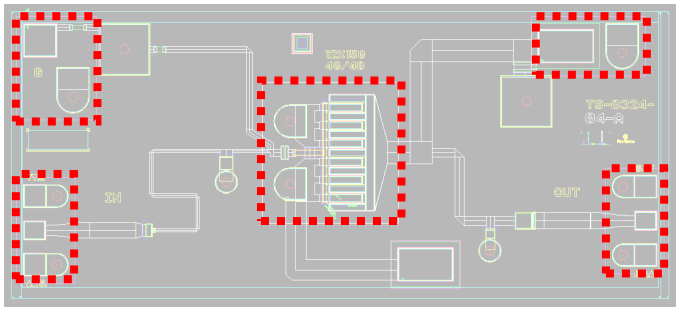


Figure 1. Designed chip with the dotted red area to be opened up for the LCP lamination.

To reproduce wafer level processing, four test chips were first mounted on a gold coated plate as shown in Figure 2. The fabrication mimics the wafer level processing of the die with laminated liquid crystal polymer overlay. A 25 micron thick LCP was first micro-machined with laser to the appropriate dimensions to the FET and bond pad areas. The micromachining was done with the formation of a laser mask which mimics the actual position of the opening with respect to the location of the chips. Since chips were placed without precise alignment, the laser mask needed to be made for each plate. The location of the pads were measured under the microscope and converted to a laser mask as shown in Figure 3.

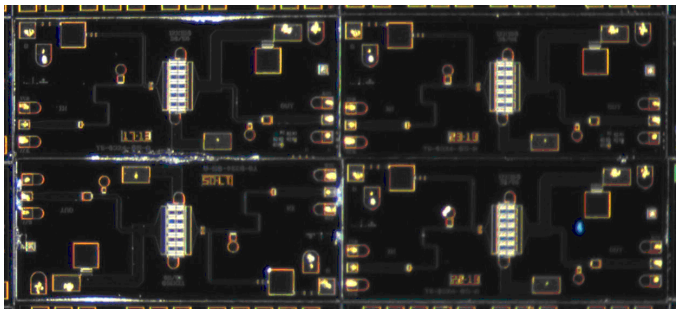


Figure 2. A photograph of 4 test chips on a carrier plate

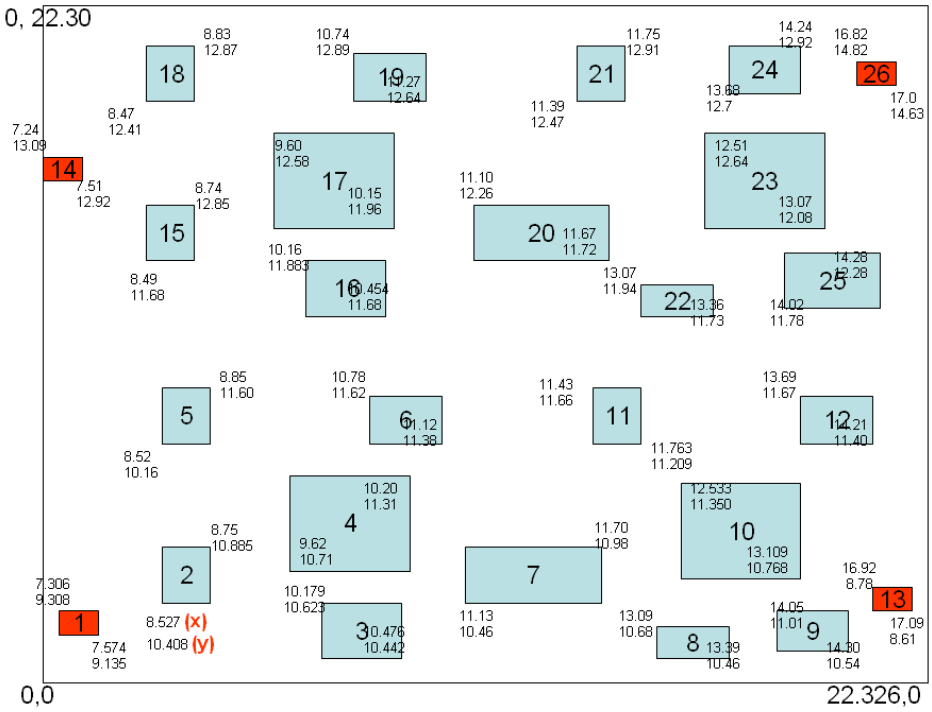


Figure 3. Opening for bond pads and FETs in the four chip plate shown in Figure 2

The micro-machined cavities were aligned to match the bond pads on the chips that are pre-mounted on the gold plate. The LCP was laminated to the wafer a pressure of 100 psi and at temperature of 270^{o}C for 30 minutes in a lamination press. The temperature, residence time, and lamination pressure were optimized to yield good interfacial bonding with high process yield. A schematic of the wafer level LCP lamination process with laser drilled cavities on the LCP is shown in Figure 4.

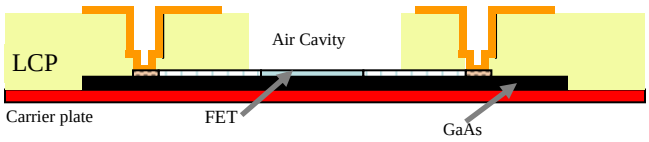


Figure 4. A schematic of the wafer level process

Experimental results

The RF performance of the chips was measured before and after the LCP lamination with the pre-cut windows over the FET area. The measured performances of a representative LNA before and after the LCP laminations are shown in Figures 5a through 5d. Several measurements were performed and the data showed good uniformity both for the control chips as well as the chips after LCP overlay.

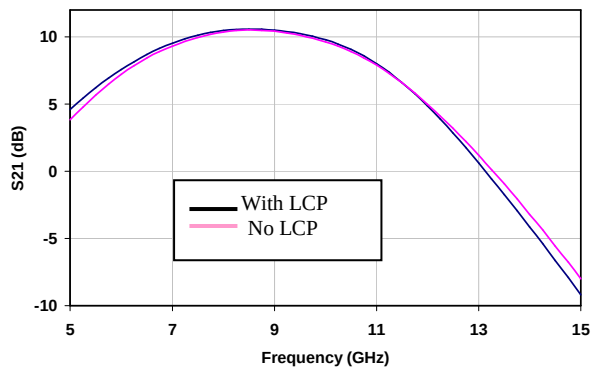


Figure 5a. S21 before and after LCP lamination

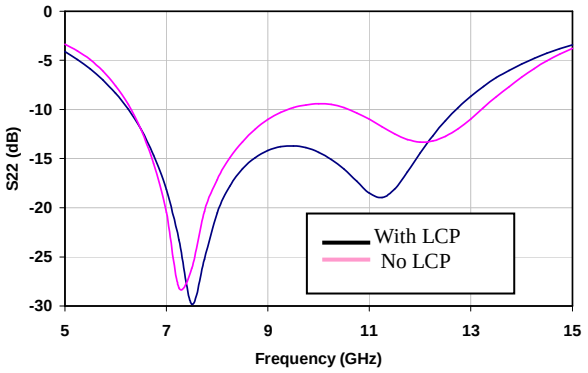


Figure 5b. S22 before and after LCP lamination

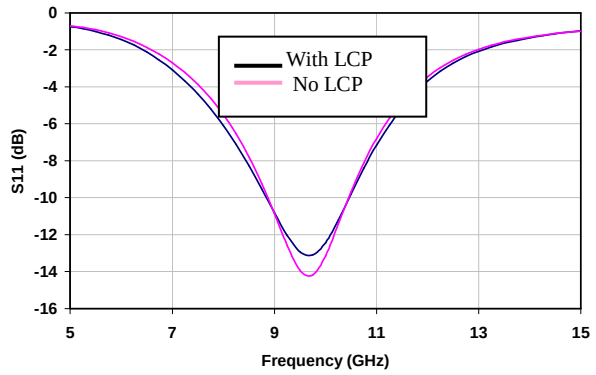


Figure 5c. S11 before and after LCP lamination

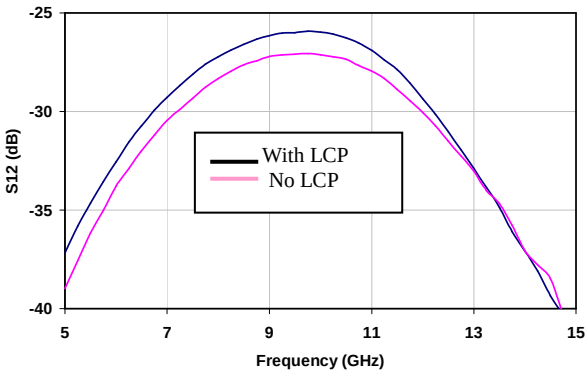


Figure 5d. S12 before and after LCP lamination

The gain of the MMIC (Figure 5a) is about 10.5 dB which peaks around 9 GHz with a bandwidth of 1 GHz. As shown in the figure 5a, the LCP coating does not degrade the gain nor shift the frequency band. Figure 5b and 6c show input and output reflection coefficients with better than 10 dB return loss within the band. The placement of the LCP had practically negligible impact on S11 and S22. This is because LCP's low dielectric constant has minimal loading on the circuits. The reverse isolation is shown in Fig. 5d. It is clear that LCP coating does not comprise the isolation of the circuit. In other words, no surface wave coupling is generated by the LCP layer.

Conclusions

A new wafer level packaging technique that combines thin, low cost organic layers with high performance MMICs has been investigated in this section. A GaAs-based single stage amplifier covered with layers of a low loss Liquid Crystal Polymer (LCP) organic material. The LCP layers allow the precise fabrication of small vertical (3-D) interconnects between the organic and semiconductor substrates with minimal loss. It was observed that the RF performance of the MMIC is virtually unaffected by this technique unlike conventional packaging processes that degrade the RF performance due to the overlay of the dielectric material on the MMIC.

Section II. Lamination DOE for Non-concaving Air Cavity in GaAs/BCB/LCP laminate

In this sub-task, formation and seating of air cavities within selected areas in the MMIcs have been explored. Unlike previous section, cavity is formed on spun on BCB using photolithography which would be covered with the LCP. Hence the critical factors are to form an effective bonding between LCP and BCB surface and keeping the LCP flat (without concaving into the cavity) after lamination.

Lamination of LCP on BCB layers for GaAs/Si Wafers

The goal of this project is to explore fundamental fabrication techniques that will eventually allow the development of a three-dimensional RF circuit as presented in Figure 6.

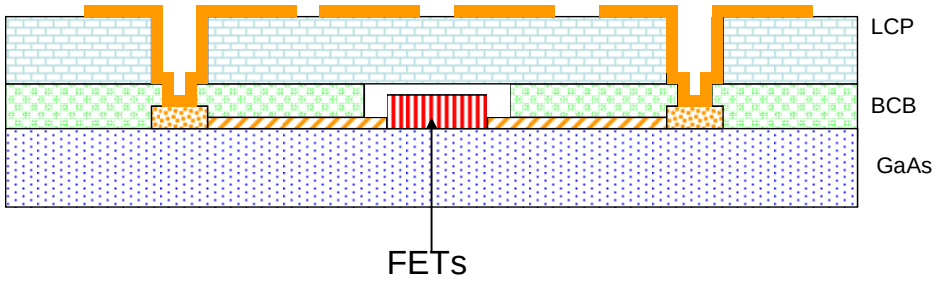


Figure 6. Conceptual drawing of a 3-D RF structure.

Experimental

Materials

Substrate Choice
- Si wafer
- GaAs Wafer

Surface Treatment
- No adhesion promoter
- Adhesion promoter and SiN

BCB
- 6 to 10 micron thick spin on
- Un-patterned and Patterned

LCP
- 4 mil thick
- Copper removed by metal etching
- RIE etch to make surface activated prior to bonding

Equipment

(1) Standard lamination press with programmable heating and cooling (Figure 7)
Platen size 14 inch x 14 inch
Minimum load 1000 lbs
Maximum load 25000 lbs

(2) Standard wafer bonder, Karl Suss SB 6 (Figure 8)
Plated size 4 inch
Maximum pressure 40 psi

Figure 7. Lamination Press

Figure 8. Karl Suss wafer bonder

Lamination Approaches

Lamination Press

The following three approaches depicted in Figure 9 are proposed for process optimization using a lamination press. The experimental procedure is described below.

The silicon wafer with spun on and soft cured BCB supplied by Raytheon was first diced (scored) into two pieces. A 4 mil thick LCP was cleaned with acetone and isopropyl alcohol and dried in air. The LCP after drying was RIE etched in oxygen for 5 minutes using a Plasmatherm RIE. The LCP sample was then washed to remove any debris from the RIE etching. After drying, the LCP sample was placed on the silicon wafer with the etched surface in contact with the soft cured BCB and gently pressed by hand. The assembly was then placed on a stainless steel mold for lamination at higher temperature and pressure using a standard hot press shown in Figure 10. Various temperature and pressure cycles were implemented for process optimizations

which are captured in Table 1. The pressure was raised first at room temperature and then temperature cycle was applied in three segments.

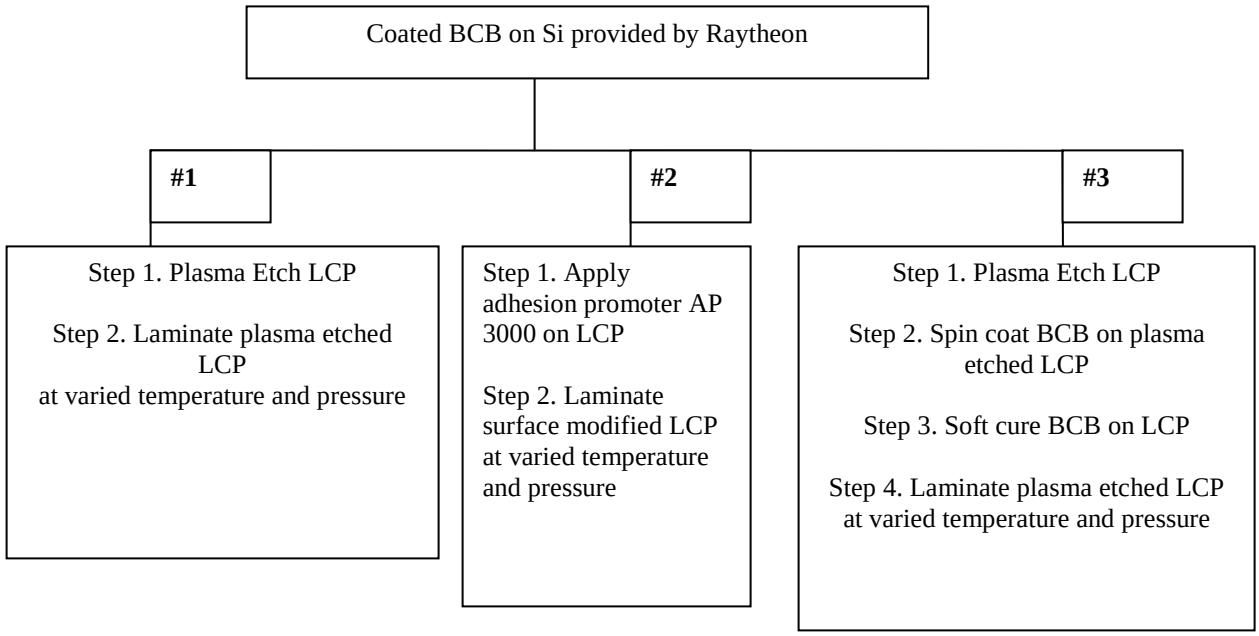
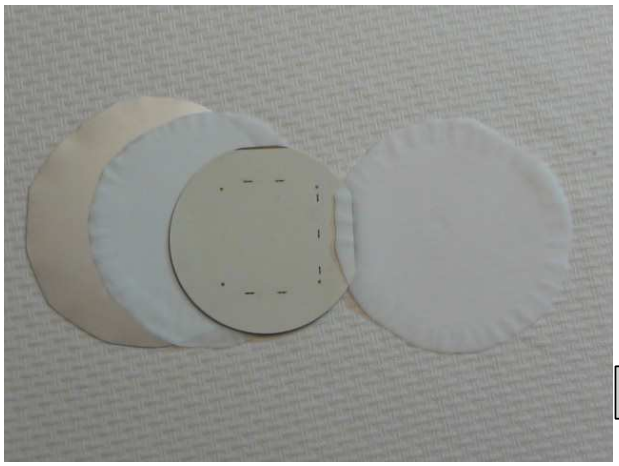


Figure 9. Approaches for bonding LCP to BCB through lamination and heat cycle.



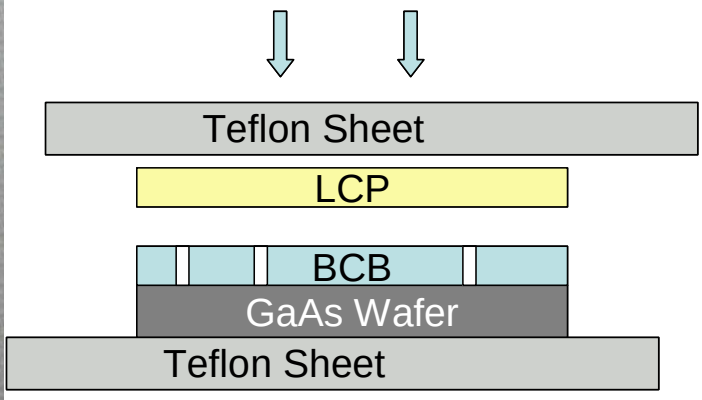


Figure 10a. Layout before lamination Figure10b. Sample fixture inside the lamination press

Wafer Bonder

A wafer bonder was also used for lamination at lower pressure. The profile for BCB cure is shown in Figure 11.

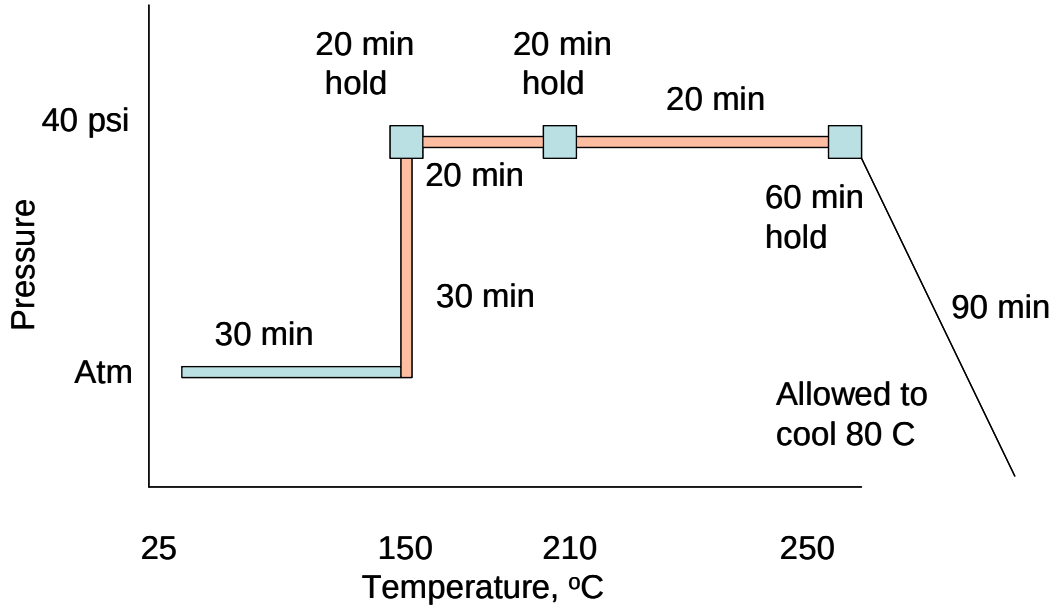


Figure 11. Lamination profile in a wafer bonder

Peel test

The adhesion strength at the interface of the BCB and LCP was tested with a tape test often used for quick assessment. The tape test confirms a peel strength of at least 0.7 kgf/cm. An accurate peel testing of the LCP/BCB interface is conducted using an Instron machine. Figure 11 shows the geometry for the peel testing. Peel tests were conducted using an Instron at 0-180^{o} configuration at 1 cm/min strain rate. The composite lamination was sectioned to approximately 1 inch width for peel testing. Results from various experiments are summarized in Table 1.

Figure 13 shows a typical load vs time (extension) curve from the Instron peel test. The sample after the test was examined in an optical microscope and the fracture surface corresponding to the load is presented within the figure. Both adhesive and cohesive failure modes were observed as represented in the micrographs. Adhesive failure at the LCP/BCB interface resulted in the highest peel test as shown in Table 1.

Reliability testing

For reliability testing, 85^{o}C/85% humidity was adopted. Samples were placed in the reliability chamber for 50 hours and 300 hours. The peel tests upon completion of the T/H cycle showed 1 kgf/cm average peel test which is higher than the standard value of 0.7 kgf/cm.

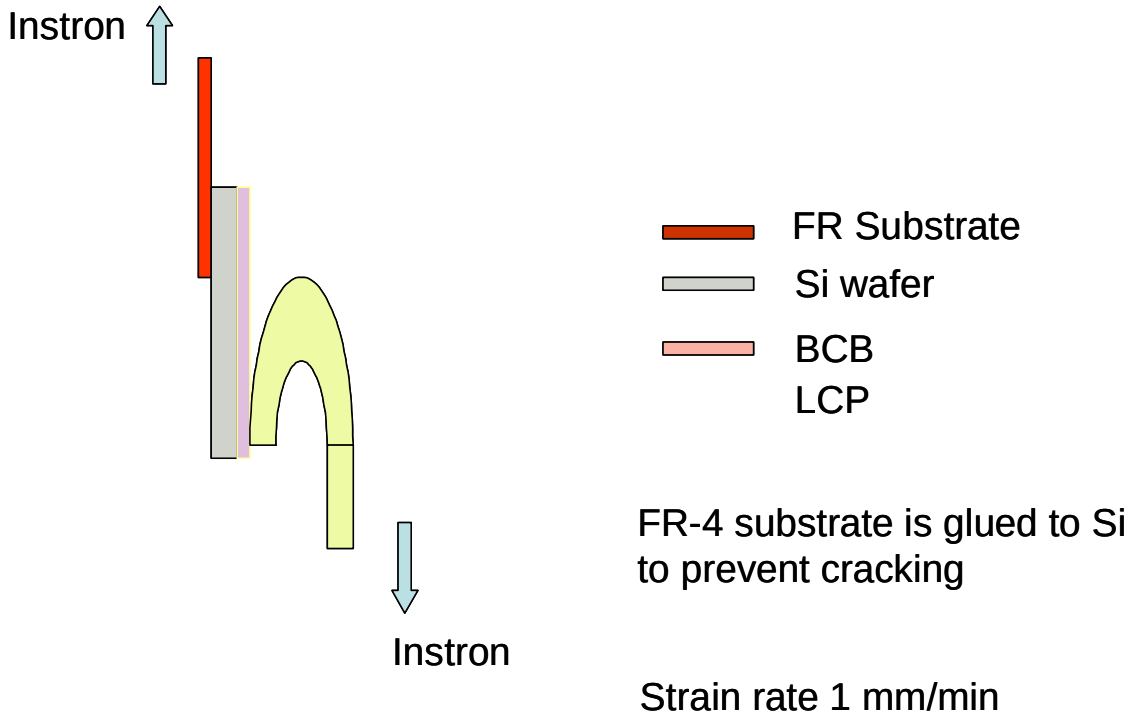


Figure 12. Peel testing configuration

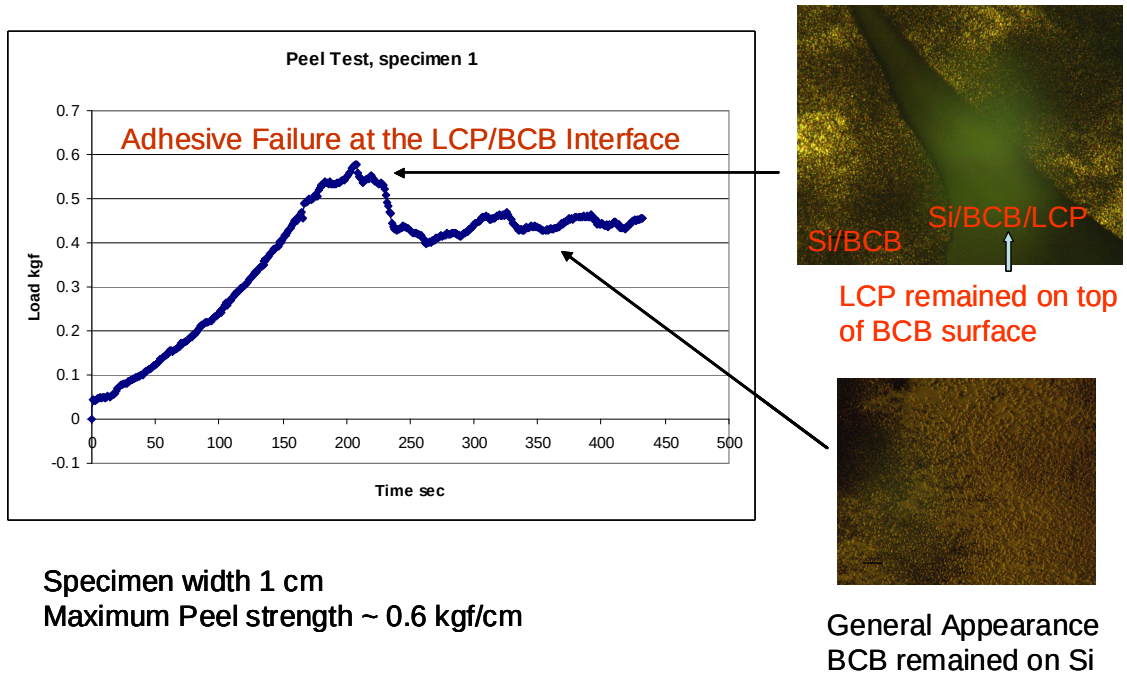


Figure 13. Load vs extension curve in peel test with micrographs of the fractured surface

Table 1. LCP/BCB Lamination Trials

Sample ID	Wafer	BCB	Tool	Pressure at 25 C	Pressure/ Time (min) at 150 °C	Pressure/ Time at 210 °C	Pressure/ Time at 250 °C	Results, LCP/BCB adhesion	Peel Test
1	Si	Blanket	Bonder	50 psi	50 psi 60 min	-	-	None	
2	Si	Blanket	Bonder	50 psi	50 psi 60 min	50 psi 60 min	-	Somewhat better	
3	Si	Blanket	Bonder	50 psi	50 psi 45 min	50 psi 60 min	50 psi 60 min	Better than #2	
4	Si	Blanket	Lamin-ation	125 psi	50 psi 45 min	50 psi 30 min	50 psi 60 min	Good	
5	Si	Blanket	Bonder	40 psi	40 psi 45 min	40 psi 60 min	40 psi 60 min	Bonded better at edge	Max 0.6 kgf/cm
6	Si	Blanket	Bonder	40 psi	40 psi 45 min	40 psi 60 min	40 psi 60 min	Bonded better at edge	
7	GaAs Sin/AP	Patterned	Bonder	38 psi	38 psi 45 min	38 psi 30 min	38 psi 60 min	Bonded better at edge	
8	GaAs Sin/AP	Patterned	Bonder	38 psi	38 psi 45 min	38 psi 30 min	38 psi 60 min	Bonded better at edge	
9	GaAs Sin/AP	Patterned	Bonder	None	None 45 min	38 psi 30 min	38 psi 60 min	Bonded better at edge	Max 0.3 kgf/cm
10	GaAs Sin/AP	Patterned	Bonder	None	None 45 min	None 30 min	38 psi 30 min	Bonded better at edge	
11	Si	Blanket, plasma etched	Bonder	None	38 psi 45 min	38 psi 30 min	38 psi 30 min	Bonded better at edge	
12	GaAs SiN/AP	Blanket	Lamina-tion	None	20 min	80 psi 30 min	80 psi 45 min	Sample broke	Not tested
13	GaAs SiN/AP	Blanket	Lamina-tion	None	20 min	80 psi 30 min	80 psi 45 min	Well bonded	1.2 kgf/cm max
14	GaAs SiN/AP	Blanket	Spray epoxy on cured BCB	1 psi	1 psi 30 min	None	None	Well bonded	1 kgf/cm Maximum

Summary and Conclusions

Several approaches have been undertaken to yield better adhesion strength and low concavity of the LCP film attached to the BCB. Below are the key observations from the various lamination studies:

Lamination Press

Better bonding
Better Uniformity
Higher pressure (80 psi)
Better peel strength > 1 kgf/cm max, 0.6 kgf/cm average
Measurements on un-patterned wafers

Low lamination pressure
Better concavity on LCP (1 to 2 micron)
Poor adhesion LCP to BCB

Higher lamination pressure
Higher concavity (1.5 to 5 micron)
Better adhesion

Wafer Bonder

Bonding better at the edge
Less Uniformity
Low peel strength, max 0.6 kgf/cm, average 0. 4 kgf/cm
Long cycle time
Lower pressure <35 psi

Section III. Via Processing

This section deals with via formation for the layer to layer Z-interconnections. The objectives are to determine the size and aspect ratio of the vias that can be formed on blank LCP, via filling by sputtering and loss per via interconnect up to at least 15 Ghz.

Vias are needed for layer to layer interconnections. A back to back transition of CPW to microstrip and microstrip to CPW design is shown in Figure 14. The vias were formed on a 4-mil LCP substrate with diameters of 50, 100 and 200 microns. An excimer laser was used for via ablation. The LCP thickness was 100 micron which showed well defined vias with 50 micron diameters. With reduced LCP thickness, smaller vias are possible. The samples after via ablation were evaporated with a Ti (200A) and Coper (5 micron) using DC sputterer. The CPW lines were fabricated with lithography. Good front to back connections was noted with a DC test showing vias were filled and well connected by DC sputter. These vias will be filled by plating which is expected to yield much better Z-interconnect with improved performance.

Measurement data up to 16 GHz is shown in Figure 15. Measurements were done using a network analyzer probing both sides of the CPW. In order to avoid the metal chuck in contact to the back plane, the sample was placed on a thin card board with empty air channels to minimize the dielectric effects on the microstrip lines. The insertion loss for the 100 micron vias was minimal through the entire frequency band (1-16 GHz) as can be seen from the comparison of a thru-line (black line) with the same total length as the line with the 3-D transitions. The 50 micron vias show 0.1 dB loss per transition.

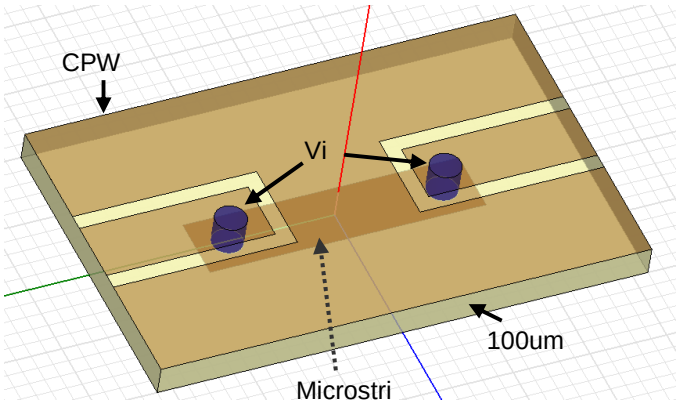


Figure 14. CPW to microstrip transitions

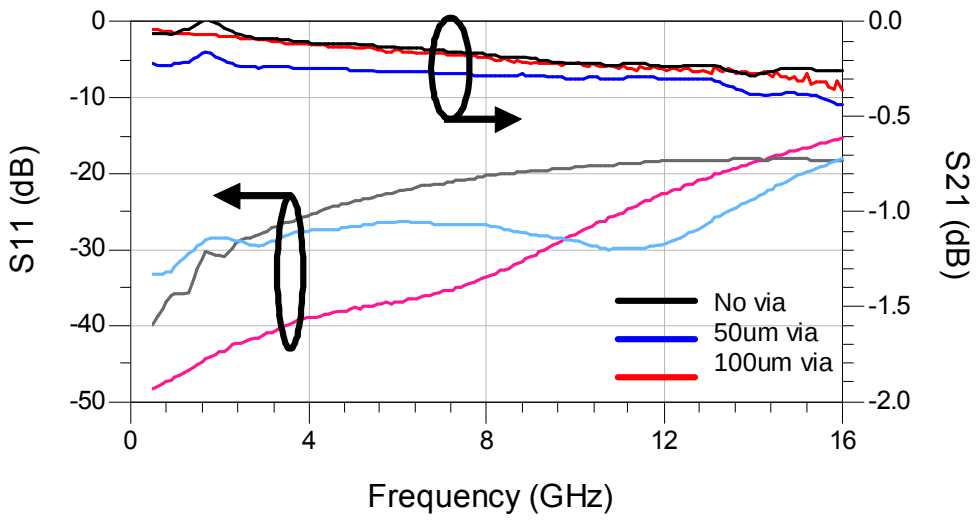


Figure 15. Insertion and return loss comparison of CPW to microstrip transition with and without vias

Conclusions

Embedded MMIC can be routed to outer layers of high performance organic layers (LCP) through opening and filling of low-loss vias. The filled vias showed virtually no additional loss from 1 to 16 GHz compared to the transmission lines with no vias. The hybrid integration process also includes the creation of air-cavities to maximize the performance of the MMICs embedded in LCP layers.

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